REMARKS

The Examiner is thanked for his careful and very thorough Office Action.

Claims 1-40 have been rejected.

Note that the amendment to Claim 29 is intended to be a purely formal amendment, and is believed not to change the scope of this claim.

The foregoing amendments to the specification are submitted to improve clarity, and to remove various typographical and other minor informalities. These changes are respectfully asserted not to introduce new matter, and their entry is respectfully requested.

Art Rejections

The art rejections are all respectfully traversed.

Review of the References

Baldwin (U.S. Patent No. 6,025,853) relates to a graphics processing chip which uses a deep pipeline of multiple asynchronous units, separated by FIFO's, to achieve a high net throughput in 3D rendering. This patent does not disclose a memory interface which provides a high bandwidth interface independent of the serial message-passing interface directly to a memory that is capable of storing displayable pixel information.

Manze et al. (U.S. Patent No. 5,675,826) relates to an image data value storage system.

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If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out very specifically where such teaching may be found.

Rejections Under 35 USC 102(b)

Claims 1, 3, 9, 13, 17, 21, 25, 29, 33, and 37 stand rejected as being anticipated by *Baldwin*.

The claim language of Claim 1 is not met. Specifically, Claim 1 recites "**a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information**".

The Examiner has suggested that the high bandwidth interface to memory disclosed by the present application is found in *Baldwin*. However, this is incorrect. The section of *Baldwin* that describes the Host Framebuffer Bypass (beginning in col. 21, line 53) does not appear to contain any suggestion that the host framebuffer bypass is a high bandwidth interface.

In contrast, the present application discloses a memory that is 256 bits wide physically, and with DDR memory, it appears to be 512 bits wide. Each access now returns sufficient data for multiple pixels. Optimizing high bandwidth with a memory architecture where memory is organized in tiles allows the architecture to accesses multiple byte-sized tiles of pixels simultaneously and not one pixel at a time. Displayable pixel information now can be stored directly to a memory associated with the graphics accelerator.

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Having this architecture gives the present invention real and technical advantages. As stated in the present application:

> ...[T]he present architecture transmits pixel data through a different high-bandwidth bus path, which provides for much greater overall fill rate. The combination of message-passing control architecture with extremely high-bandwidth to memory provides a further improvement over the GLINT architecture[1]...
>
> Some observations contrasting this architecture to earlier ones of 3Dlabs:
>
> The message stream does not visit every unit.
>
> Trying to route a linear message stream though the texture pipes is fairly problematic, although fanning it out like in Gamma 3 would have been an option.
>
> It turns out that the texture units in the texture pipe have little or no state or any need for the color and coordinate information, but are heavily pipelined or have deep latency

[1] Paragraph [0032].

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FIFOs. Not forcing the message stream to be routed through them saves on pipeline register and FIFO widths.

The only down side is in testing as the interfaces are not so uniform across units.

The message stream does not carry any pixel data except for upload/download data and fragment coverage data.

The private data paths give more bandwidth and can be tailored to the specific needs of the sending and receiving units.

The private data path between the Shading Unit (via the Texture Mux Unit) and Pixel Unit doesn't need to go through the Router, or any other unit. If the message stream were increased in width to give the required bandwidth then the cost would be borne in a number of places. It will be necessary to have it FIFO buffered, particularly when the Router places the texture

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> subsystem first so that texture processing is not stalled while waiting for the Pixel Unit to use its data, but this cannot happen until the Tile message has reached it. Having one FIFO doing this buffering will be a lot cheaper than a distributed one and will ease chip layout routing.
>
> The message stream is still the only mechanism for loading registers and synchronizing internal operations.[2]

Of course, this text of the specification is cited for the purpose of distinguishing the present inventions from the applied reference, and does not define the scope or interpretation of any of the claims, which speak for themselves. Accordingly, *Baldwin* does not appear to disclose or suggest the high bandwidth memory interface of the present application or the corresponding advantages.

According to the Federal Circuit:

> For a prior art reference to anticipate a claim, the reference must disclose each and every element of the claim with

[2] Paragraphs [0079-0087].

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sufficient clarity to prove its existence in the prior art.[3]

Therefore, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 1.

The claim language of Claim 3 also is not met. Specifically, Claim 3 recites "**a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information**".

As stated above, *Baldwin* does not appear to disclose a high bandwidth memory interface independent of the serial message-passing interface that interfaces with a memory capable of storing displayable pixel information. Therefore, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 3.

The claim language of Claim 9 also is not met. Specifically, Claim 9 recites "**a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information**".

Again, *Baldwin* does not appear to disclose a high bandwidth memory interface independent of the serial message-passing interface that interfaces

[3] Motorola, Inc. v. Interdigital Tech. Corp., 43 USPQ 2d 1481, 1490 (Fed. Cir. 1997).

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directly with a memory capable of storing displayable pixel information. Accordingly, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 9.

The claim language of Claim 13 also is not met. Specifically, Claim 13 recites "**a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information**".

Again, *Baldwin* does not appear to disclose a high bandwidth memory interface independent of the serial message-passing interface that interfaces with a memory capable of storing displayable pixel information. Accordingly, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 13.

The claim language of Claim 17 also is not met. Specifically, Claim 17 recites "**a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information**".

As established above, *Baldwin* does not appear to disclose a high bandwidth memory interface independent of the serial message-passing interface that interfaces directly with a memory capable of storing displayable pixel information. Accordingly, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 17.

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The claim language of Claim 21 also is not met. Specifically, Claim 21 recites "**a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information**".

As established earlier, *Baldwin* does not appear to disclose a high bandwidth memory interface independent of the serial message-passing interface that interfaces directly with a memory capable of storing displayable pixel information. Accordingly, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 21.

The claim language of Claim 25 also is not met. Specifically, Claim 25 recites "**providing a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator through a memory interface, said memory capable of storing displayable pixel information**".

Again, *Baldwin* does not appear to provide for a high bandwidth memory interface independent of the serial message-passing interface that interfaces directly with a memory capable of storing displayable pixel information. Therefore, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 25.

The claim language of Claim 29 also is not met. Specifically, Claim 29 recites "**providing an interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator**

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through a memory interface, said memory capable of storing displayable pixel information".

As established above, *Baldwin* does not appear to provide for a memory interface independent of the serial message-passing interface that interfaces directly with a memory capable of storing displayable pixel information. Therefore, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 29.

The claim language of Claim 33 also is not met. Specifically, Claim 33 recites "**a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a memory associated with said graphics accelerator, said memory capable of storing displayable pixel information**".

As stated above, *Baldwin* does not appear to provide for a high bandwidth memory interface independent of the serial message-passing interface that interfaces directly with a memory capable of storing displayable pixel information. Therefore, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 33.

The claim language of Claim 37 also is not met. Specifically, Claim 37 recites "**a high bandwidth memory interface independent of said serial message-passing interface which interfaces directly to a memory of said graphics accelerator, said memory capable of storing displayable pixel information**".

Again, *Baldwin* does not appear to provide for a high bandwidth memory interface independent of the serial message-passing interface that

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interfaces directly with a memory capable of storing displayable pixel information. Therefore, a prima facie case of anticipation has not been established by the Examiner with regard to Claim 37.

Accordingly, for the reasons stated above, Applicant submits that each independent claim is patentably distinct from *Baldwin* and respectfully requests withdrawal of this rejection.

Rejections Under 35 USC 103(a)

Claims 2, 4-8, 10-12, 14-16, 18-20, 22-24, 26-28, 30-32, 34-36, and 38-40 stand rejected as being unpatentable over *Baldwin* in view of *Manze et al.*

With regard to Claims 2, 4, 10, 14, 18, 22, 26, 30, 34, and 38, the Examiner has noted that *Baldwin* fails to explicitly teach or suggest the memory interface accessing multiple tiles of pixels simultaneously. The Examiner has suggested that it would have been obvious to combine the teachings of *Manze et al.* into the system of *Baldwin* in order to simultaneously access multiple memory blocks in the tiled memory unit and thus to provide improved access to larger arrays of pixel data. However, merely stating a logical result of the suggested combination is hindsight reconstruction, not motivation.

According to the Federal Circuit:

> **Determination of obviousness can not be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention. There must be a teaching or suggestion within the prior, or**

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> **within the general knowledge of a person of ordinary in the field of the invention, to look to particular sources of information, to select particular elements, and to combine them in a way they were combined by the inventor.**[4]

Accordingly, the Examiner has failed to establish a proper motivation for the suggested combination.

Also, dependent Claims 2, 4, 10, 14, 18, 22, 26, 30, 34, and 38 depend directly from allowable independent Claims 1, 3, 9, 13, 17, 21, 25, 29, 33, and 37 and incorporate all the limitations thereof. As established above, the claim language of each of these allowable independent claims is not met. Therefore, even if one were motivated to make the suggested combination, which Applicant strongly disputes, it still would not support each limitation of these dependent claims.

As determined in *Thrift,*[5] a rejection which "does not discuss the unique limitations" of the claims was held to be "simply inadequate on its face." In this case, a rejection was held "not supported by substantial evidence because **the cited references do not support each limitation** of claim 11." See *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1443 (Fed.Cir. 1991)."[6] Therefore, a prima facie case of obviousness has not been established by the Examiner with regard to these dependent claims.

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[4] *ATD Corp. v. Lydall, Inc.*, 48 USPQ 2d 1321, 1329 (Fed. Cir. 1998).

[5] *In re Thrift*, 298 F.3d 1357 (Fed.Cir. 2002).

[6] *In re Thrift*, 298 F.3d at 1366 (emphasis added).

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With regard to Claims 5, 7, 11, 15, 19, 23, 27, 31, 35, and 39, the Examiner has noted that the asserted combination fails to explicitly teach or suggest the size of the tiles of pixel. The Examiner has suggested that it would have been obvious to modify the teachings of the applied references in order to provide the design size (or shape) of the tiles of pixel in order to add flexibility and performance to the system. Once again, merely stating a logical result of the suggested combination is hindsight reconstruction, not motivation. Accordingly, the Examiner has failed to establish a proper motivation for the suggested combination.

Also, dependent Claims 5, 7, 11, 15, 19, 23, 27, 31, 35, and 39 depend directly from allowable independent Claims 1, 3, 9, 13, 17, 21, 25, 29, 33, and 37 and incorporate all the limitations thereof. As established above, the claim language of each of these allowable independent claims is not met. Therefore, even if one were motivated to make the suggested combination, which Applicant strongly disputes, it still would not support each limitation of the above dependent claims. Therefore, a prima facie case of obviousness has not been established by the Examiner with regard to these dependent claims.

With regard to dependent Claims 6, 8, 12, 16, 20, 24, 28, 32, 36, and 40, these claims depend directly from allowable independent Claims 1, 3, 9, 13, 17, 21, 25, 29, 33, and 37 and incorporate all the limitations thereof. As established above, the claim language of each of these allowable independent claims is not met. Therefore, even if one were motivated to make the suggested combination, which Applicant strongly disputes, it still would not support each limitation of the above dependent claims. Therefore, a prima facie case of obviousness has not been established by the Examiner with regard to these dependent claims.

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Conclusion

This amendment is being submitted in response to the Final Office Action dated 01/16/2004 and, therefore, could not have been submitted earlier. Its entry is respectfully requested. All grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Robert Groover for an interview to resolve any remaining issues.

Respectfully submitted,

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